

ABSTRACT

A method and an apparatus for power management in a computer system have been disclosed. One embodiment of the method includes monitoring transactions over an interconnect coupling a chipset device and a peripheral device in the system, the transactions being transmitted between the peripheral device and the chipset device according to a flow control protocol to allow the chipset device to keep track of the transactions, and causing a processor in the system to exit from a power state if a plurality of coherent transactions pending in a buffer of the chipset device exceeds a first threshold. Other embodiments are described and claimed.